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THE POWER FACTOR CORRECTION IMPROVEMENT FOR A SINGLE PHASE AC/DC CONVERTER USING AN ENABLING WINDOW CONTROL

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ABSTRACT

With the rapid development in the power electronics devices, DC power supplies are the wide range of application, including residential, commercial, and aerospace and traction system and SMPS. Normally, the conventional continuous conduction mode boost converter has been widely used for power factor correction (PFC) applications because of its high input power factor and simplicity, though it suffers from conduction loss in the input rectifier bridge and switching loss due to the high switching frequency. The efficiency decreases rapidly under the lower input voltage or the light-load work condition. In this paper, a novel Enabling Window Control (EWC) method is used to reduce the switching loss and to improve the efficiency. Moreover, electromagnetic interference noise and driving loss of the main switch can be reduced with the EWC method. And also we discuss and compare some of the dc/dc converters like buck, boost, buck-boost, cuk and sepic with and without using EWC method. Simulation results are obtained in the MATLAB/SIMULINK for the effectiveness of the study.

***KEYWORDS*: Diode Bridge, Boost Power Factor Correction, Boost PFC Topologies, Enabling Window Control (EWC) & Hysteresis Current PWM**

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Original Article

I. INTRODUCTION

Power factor correction (PFC) used as a basic requirement for power electronics devices. The Figure 1 shows the conventional boost converter with continuous conduction mode (CCM),which is the most popular topologies for PFC applications due to near unity power factor, continuous input current, and electromagnetic interference (EMI) filter size is small [1] – [3]. However, in the light-load work condition or under low input voltage of CCM boost converter, the efficiency is poor because of the higher conduction loss of the input rectifier bridge and higher switching loss [4] – [6].

The switching loss is proportional to the switching frequency, and efficiency will be improved with the decrease of switching frequency. However, lower switching frequency may cause a higher current ripple of the input filter, zero-crossing distortion, and lower power factor. Many methods have been proposed regarding the tradeoff between the power factor and efficiency.

The line-frequency switching method has been used for the PFC converter to reduce the switching loss [7] – [12]. The switch is turned ON and OFF only twice in a line cycle; thus, the switching loss is reduced compared

with the high-frequency switching boost PFC. However, it needs a larger inductor and the output voltage cannot be regulated tightly with wide load [13]. A similar asymmetric pulse width modulation (PWM) with double line-frequency switching method was proposed to further reduction in the harmonic distortion, and an extra conduction time of the main switch was added to increase the conduction time of the input current [14]. A partial active PFC technology has been presented by integrating active bridgeless PFC and passive PFC [15]. The switch remains in the OFF - state in certain duration of the half-line cycle, while the switch is still operating at higher switching frequency in the remaining period of the half-line cycle. The switching loss is reduced due to fewer switching cycles. However, only step-down output voltage can be achieved with the partial active PFC and the output voltage cannot be regulated tightly with wide load variations.

The conduction loss of the diode bridge is the disadvantage of the losses. Many topologies have been introduced to reduce the conduction loss of the rectifier bridge. Bridgeless PFC generates less conduction loss compared with the conventional boost PFC (CB PFC), since there are only two voltage drop of semiconductors in the current path [16] – [18]. Voltage double PFC also has only two voltage drop of semiconductors in the current path, but the output voltage should be twice the peak of input voltage.

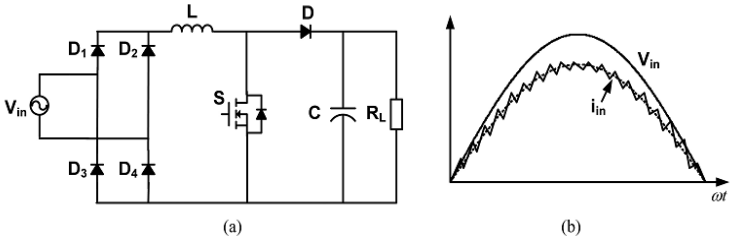

Figure 1: CCM Boost PFC
(a) Topology of CCM Boost PFC
(b) Waveforms of CCM Boost PFC

In this paper, a proposed Enabling Window Control (EWC) is introduced to reduce the switching loss. In the PFC circuit, in the middle area of a half-line cycle most of the power is transferred where the input voltage is higher. Hence, to reduce the switching loss at lower switching frequency is used in this area. In the other areas of a half-line cycle, less power is transferred and the switching loss is also less. However, it is difficult to track the sinusoidal reference signal with a lower switching frequency. Therefore, a higher switching frequency, such as 100 KHz, is used in these areas to avoid zero point distortion and achieve a high power factor. The proposed EWC method is easy to implement with existing PFC ICs, and only a few additional control components are needed. The efficiency is improved, EMI noise and driving loss of main switch can be reduced with EWC method. With the method proposed in this paper, higher efficiency can be obtained, and the standard regulations of power factor and harmonics can be satisfied without increasing the size of the inductor. In addition, step-up output voltage with tight regulation can be achieved at the same time.

II. BLOCK DIAGRAM OF THE PROPOSED SYSTEM

The block diagram describes the proposed system is shown in the Figure 2, the proposed EWC method is used to reduce the switching losses and achieve high power factor which is near unity with two different switching frequencies. The higher efficiency can be obtained and harmonics are reduced without increasing the inductor size.

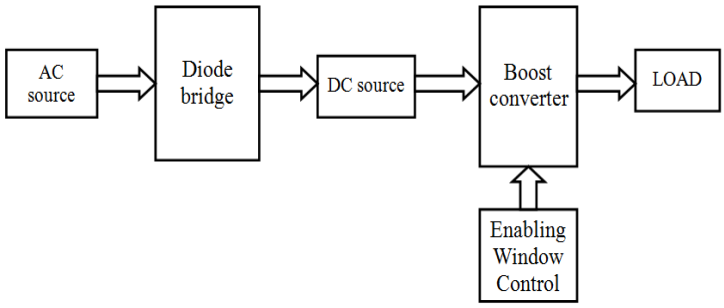

Figure 2: Block Diagram of the Proposed System

III. PRINCIPLE OF EWC

For the CCM boost PFC, the input current and voltage waveforms are in-phase sine waves, which are expressed as

$$V_{in}(t) = V_m \sin(\omega t)$$
$$I_{in}(t) = I_m \sin(\omega t) \quad (1)$$

It is assumed that the loss of the circuit is small enough that can be ignored, and then, the instantaneous input power can be described as

$$P_{in}(t) = V_m I_m \sin^2(\omega t)$$
$$= P_o(1 - \sin(\omega t)) \quad (2)$$

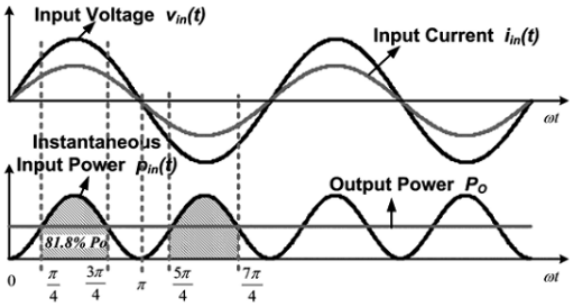

Figure 3: Instantaneous Input Power of CB PFC

Where V_m is the input voltage, I_m is the input current, P_{in} is the input power and P_o is the output power where $P_o = \frac{V_m I_m}{2}$ is shown in the Figure 3.

Most of the power is transferred during the shadow area in high-line cycle. The power transferred in the shadow area can be calculated as follows:

$$P_{shadow}(t) = \frac{1}{\pi}\int_{\frac{\pi}{4}}^{\frac{3\pi}{4}} P_{in}(\omega t)\, d(\omega t)$$
$$= \frac{1}{\pi}\int_{\frac{\pi}{4}}^{\frac{3\pi}{4}} P_o\,(1 - \cos(2\omega t))d(\omega t)$$
$$= 81.8\%P_o \quad (3)$$

Equation (3) shows that more than 80% power is transferred in the shadow area. As a result, most of power loss is generated in this area.

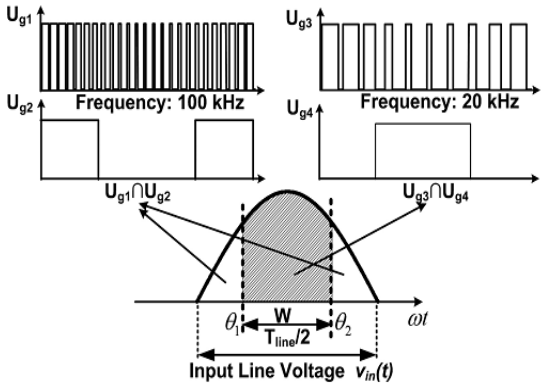

Figure 4: Principle of EWC

The principle behind the proposed EWC is proposed in the Figure 4.Here, T_{line} is the line period and W is the duration of window area. Thus, the window size can be defined as

$$k = \frac{W}{T_{line}/_2} \tag{4}$$

In a half-line cycle, mainly the power is transferred in the middle area where the input voltage is higher (see the shadow area in the Figure 4. More switching losses are generated in this area, which can be reduced significantly with the decrease of the switching frequency in this area. However, the switching frequency should be higher than 20 kHz to avoid the audio noise.

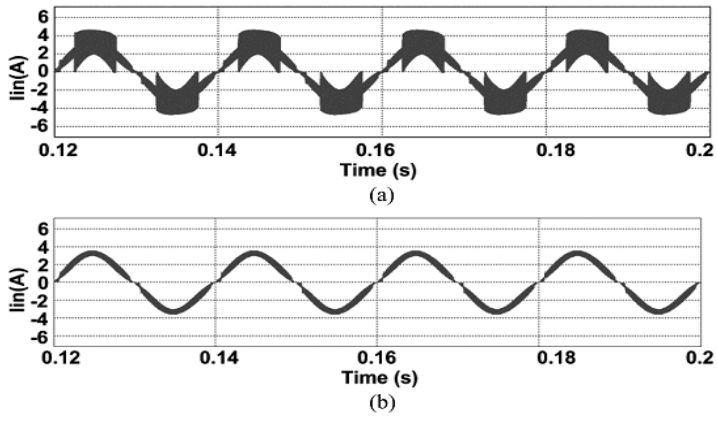

Figure 5: Input Current Waveforms of CB PFC and EWC PFC

(a) Input Current Waveforms of EWC PFC (V_{in} = 230 V_{ac}, P_O = 500 W, k = 0.5, T_{line} =20 ms)
(b) Input Current Waveforms of CB PFC (V_{in} = 230 V_{ac}, P_O = 500W, T_{line} = 20 ms)

On the outside of the shadow area, less power is transferred and the switching loss is smaller. However, it is difficult to track quick changing sinusoidal reference signal with low switching frequency which may lead to the distortion of zero crossing point and lower power factor. A high switching frequency, such as 100 kHz is used on the outside of the

shadow areas to achieve a high power factor.

The inductor plays a critical role in the boost PFC. It should be well designed with consideration of power density, efficiency, and power factor. In the CB PFC, the inductor is usually selected to ensure 20%current ripple under the lowest input voltage. The required inductance is calculated as follows:

$$L = \frac{\sqrt{2}V_{in\_min}}{I_{in\_peak}*20\%} * \frac{V_o - \sqrt{2}V_{in\_min}}{V_o} * \frac{1}{f} \quad (5)$$

I_{in_peak} is represented as follows:

$$I_{in_{peak}} = \frac{\sqrt{2}P_o}{\eta V_{in\_min}} \quad (6)$$

where $V_{in\ min}$ is the minimum input rms voltage, I_{inpeak} is the peak input current, η is the efficiency of PFC (typically0.95), and P_O is the output power. As shown in (5), the inductance is inversely proportional to the switching frequency.

IV. SIMULATION RESULTS

The values used in the simulation model for proposed method is shown in table.1:

Table 1: Simulation Parameters

PARAMETERS	VALUES
Input voltage	230Vac
Inductor	1.12mH
Capacitor	390µF
R load	100Ω
Window size	0.5

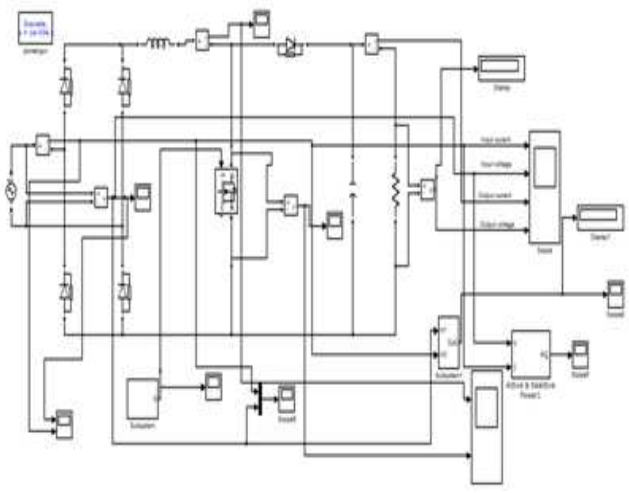

Figure 6: Simulation of the Proposed System

The Figure 6 shows the simulation model of the proposed system.

The change of switching frequency is shown in Figure 7, the switching frequency changes from 20kHz to 100kHz and 100kHz to 20kHz.

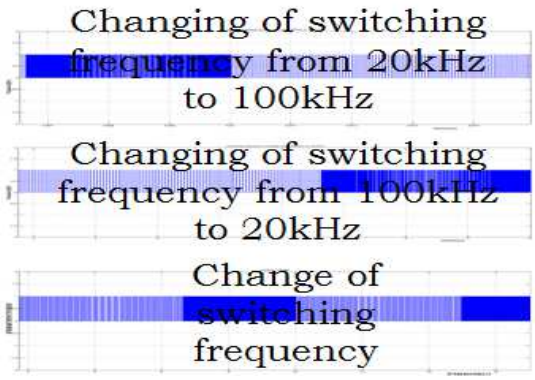

Figure 7: Change of switching frequencies

The simulation results of proposed method is shown in Figure 8

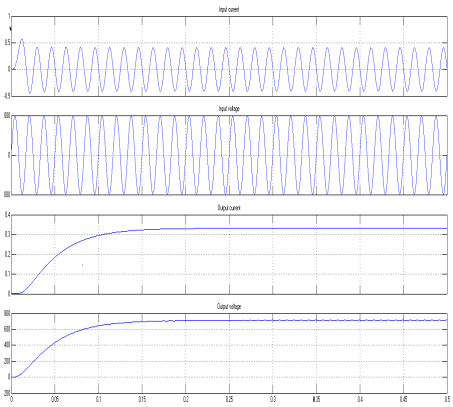

Figure 8: Simulation Result for the Proposed Method

The output voltage is stepped up to 714V and the total harmonics distortion is 0.89% and power factor reaches near unity.

The FFT analysis of proposed method is shown in Figure 9:

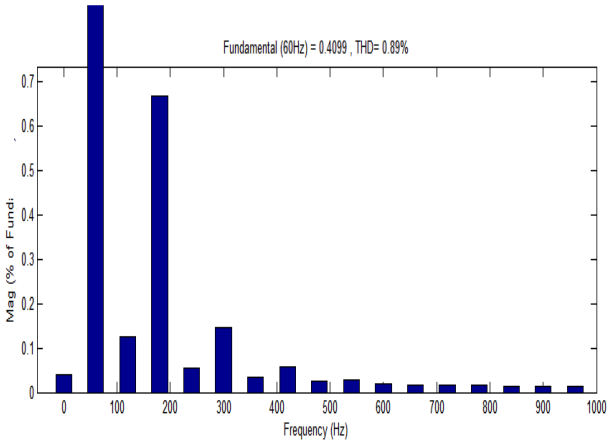

Figure 9: FFT Analysis of Proposed Method

The comparative analysis of proposed method with different PFC topologies is shown in Figure 10

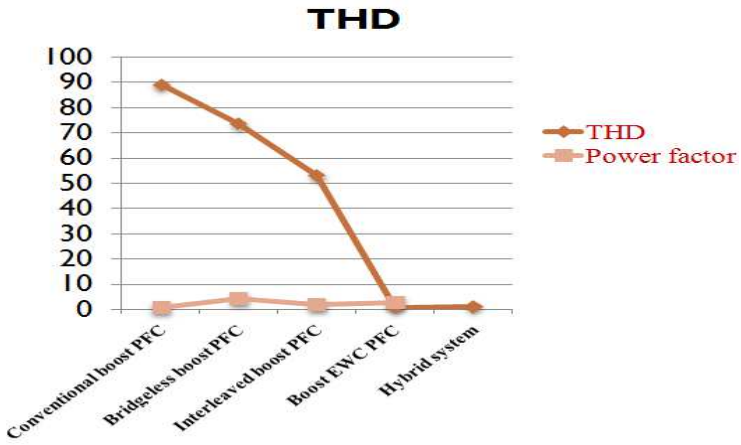

Figure 10: Comparative Analysis of the Proposed with the Different PFC Topology

V. CONCLUSIONS

This paper presents Enabling Window Control for non-linear load, in this method, switching loss is reduced, higher efficiency can be obtained, and standard regulation of power factor and harmonics can be achieved at the same time without increasing the inductor size. In addition, step-up output voltage with tight regulation can be achieved at the same time. Moreover, EMI noise and driving loss of the main switch was reduced with this method. When compared with the existing boost PFC topologies like bridgeless boost PFC and interleaved boost PFC, the total harmonic distortion is reduced and power factor reaches to 0.9999.

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